CLAIM AMENDMENTS

Claim 1-24 (canceled)

Claim 25 (currently amended) ~~The system of claim 1,~~ A system comprising:

a memory bus; and

a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a predetermined priority scheme, the predetermined priority scheme defining time slots, wherein the memory controllers are allocated to respective time slots according to the predetermined priority scheme, and at least two of the plurality of memory controllers adapted to generate concurrently pending memory requests on the memory bus in plural respective time slots;

wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

Claim 26 (canceled)

Claim 27 (currently amended) ~~The system of claim 26,~~ A system comprising:

a plurality of memory buses;

a hub connected to the plurality of memory buses; and

a plurality of memory controllers connected to a first one of the memory buses, each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions, the memory controllers to access a second one of the memory buses through the hub; and

wherein at least two of the memory controllers are adapted to generate concurrently pending memory requests on the first memory bus, each of the concurrently pending memory requests comprising control information and memory address information and, wherein one of the at least two memory controllers is adapted to

generate its memory request including control information and memory address information on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

Claim 28 (canceled)

Claim 29 (currently amended) ~~The method of claim 28,~~ A method for use in a system having plural memory buses, a hub connected to the memory buses, and a plurality of memory controllers, the method comprising:

generating requests, by the memory controllers, on the memory buses; and

each memory controller monitoring memory-related actions on the memory buses connected by the hub by at least another memory controller;

wherein generating the requests on the memory bus comprises at least two of the memory controllers generating concurrently pending requests on the memory bus, each of the concurrently pending requests comprising control information and memory address information, and wherein generating concurrently pending requests comprises one of the at least two memory controllers generating is request including control information and memory address information on the memory bus before data is returned for the request of the other of the at least two memory controllers.

Claim 30 (canceled)

Claim 31 (currently amended) ~~The system of claim 1,~~ A system comprising:

a memory bus; and

a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a predetermined priority scheme, the predetermined priority scheme defining time slots, wherein the memory controllers are allocated to respective time slots according to the predetermined priority scheme, at least two of the plurality of memory controllers adapted to generate concurrently pending memory requests on the memory bus in plural respective time slots; and

wherein the predetermined priority scheme enables the memory controllers to gain access to the memory bus without having to assert arbitration requests.

Claim 32-33 (canceled)

Claim 34 (currently amended) ~~The system of claim 33,~~ A system comprising:

a memory bus; and

a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a predetermined priority scheme, the predetermined priority scheme defining time slots, wherein the memory controllers are allocated to respective time slots according to the predetermined priority scheme, at least two of the plurality of memory controllers adapted to generate concurrently pending memory requests on the memory bus in plural respective time slots;

wherein the memory bus comprises a first memory bus, the system further comprising:

a hub connected to the first memory bus, and

a second memory bus connected to the hub, at least two of the memory controllers adapted to generate concurrently pending memory requests on the second memory bus through the hub; and

wherein each of the memory request comprises control information and memory address information, the at least two memory controllers adapted to generate concurrently pending memory requests on the second memory bus by providing control information and memory address information of the concurrently pending memory requests on the second memory bus.

Claim 35 (currently amended) ~~The system of claim 33,~~ A system comprising:

a memory bus; and

a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a predetermined priority scheme, the

predetermined priority scheme defining time slots, wherein the memory controllers are allocated to respective time slots according to the predetermined priority scheme, at least two of the plurality of memory controllers adapted to generate concurrently pending memory requests on the memory bus in plural respective time slots;

wherein the memory bus comprises a first memory bus, the system further comprising:

a hub connected to the first memory bus, and

a second memory bus connected to the hub, at least two of the memory controllers adapted to generate concurrently pending memory requests on the second memory bus through the hub; and

wherein each of the memory requests comprises control information and memory address information, the at least two memory controllers adapted to generate concurrently pending memory requests on the first memory bus by providing control information and memory address information of the concurrently pending memory requests on the first memory bus.

Claim 36 (currently amended) ~~The system of claim 10,~~ A system comprising:

a plurality of memory buses;

a hub connected to the plurality of memory buses;

a plurality of memory controllers connected to a first one of the memory buses, each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions,

the memory controllers to access a second one of the memory buses through the hub; and

wherein the plurality of memory controllers are each adapted to generate memory requests on the first one of the memory buses, each memory controller to monitor memory requests on the first one of the memory buses generated by another memory controller on the first one of the memory buses.

Claim 37 (currently amended) ~~The system of claim 10,~~ A system comprising:

a plurality of memory buses;

a hub connected to the plurality of memory buses;

a plurality of memory controllers connected to a first one of the memory buses, each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions,

the memory controllers to access a second one of the memory buses through the hub; and

wherein the plurality of memory controllers are each adapted to generate memory requests on the second one of the memory buses, each memory controller to monitor memory requests on the second one of the memory buses generated by another memory controller on the second one of the memory buses.

Claim 38 (previously presented) The system of claim 37, wherein the memory controllers are adapted to access any of the memory buses according to a time slot priority scheme that defines a plurality of time slots allocated to respective memory controllers.

Claim 39 (previously presented) The system of claim 38, wherein the memory controllers are adapted to access any of the memory buses according to the time slot priority scheme without asserting arbitration requests.

Claim 40 (canceled)

Claim 41 (currently amended) ~~The system of claim 11,~~ A system comprising:

a plurality of memory buses;

a hub connected to the plurality of memory buses;

a plurality of memory controllers connected to a first one of the memory buses, each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions that comprise a read-modify-write transaction,

the memory controllers to access a second one of the memory buses through the hub; and

wherein a first one of the memory controllers is adapted to generate the read-modify-write transaction, the first one of the memory controllers to assert a lock indication for a memory location accessed by the read-modify-write transaction to prevent another one of the memory controllers from accessing the memory location.

Claim 42 (currently amended) ~~The method of claim 15, further comprising:~~ A method for use in a system having plural memory buses, a hub connected to the memory buses, and a plurality of memory controllers, the method comprising:

generating requests, by the memory controllers, on the memory buses;

each memory controller monitoring memory-related actions on the memory buses connected by the hub by at least another memory controller;

the plurality of memory controllers generating memory requests on a first one of the memory buses; and

each memory controller monitoring memory requests on the first one of the memory buses generated by another memory controller on the first one of the memory buses.

Claim 43 (currently amended) ~~The method of claim 15, further comprising:~~ A method for use in a system having plural memory buses, a hub connected to the memory buses, and a plurality of memory controllers, the method comprising:

generating requests, by the memory controllers, on the memory buses;

each memory controller monitoring memory-related actions on the memory buses connected by the hub by at least another memory controller;

the plurality of memory controllers generating memory requests on a second one of the memory buses through the hub; and

each memory controller monitoring memory requests on the second one of the memory buses generated by another memory controller on the second one of the memory buses.

Claim 44 (canceled)